BL O/281/12

PATENTS ACT 1977

APPLICANT	Intel Corporation	
ISSUE	Whether GB 2373896B relates to the same invention as EP 1259870B1 under Section 73(2); Whether amendments filed under Section 73(2) meet the requirements of Section 76(3)(a) and 76(3)(b).	25 July 2012
HEARING OFFICER	Mr. Ben Buchanan	

DECISION

Introduction

1 Granted patent GB 2373896B ("the GB patent") and granted EP(UK) patent EP 1259870B1 ("the EP patent") have the same priority date and were filed by the same applicant, Intel Corporation. On 28th February 2011 the Comptroller notified the applicant of proceedings under section 73(2) to revoke the GB patent, and the applicant has proposed amendments in response.

2 The Examiner considered that the first amendments filed 28th June 2011 disclosed additional matter and extended the scope of protection conferred, contrary to sections 76(3)(a) and 76(3)(b). Second amendments filed 12th December 2011 were considered not to resolve the conflict with the EP patent. On 29th May 2012 a decision on the papers on file was requested, and the applicant filed further proposed amendments at the same time, which are considered here.

3 This decision relates to three issues – whether the proposed amendments filed on 29th May 2012 under section 73(2) meet the requirements of (i) section 76(3)(a) and (ii) section 76(3)(b), and (iii) whether the proposed amendments to the GB patent define the same invention as the EP patent.

The law

4 Section 73(2) of the Patents Act states:

> *If it appears to the comptroller that a patent under this Act and a European patent (UK) have been granted for the same invention having the same priority date, and that the applications for the patents were filed by the same applicant or his successor in title, he shall give the proprietor of the patent*

under this Act an opportunity of making observations and of amending the specification of the patent, and if the proprietor fails to satisfy the comptroller that there are not two patents in respect of the same invention, or to amend the specification so as to prevent there being two patents in respect of the same invention, the comptroller shall revoke the patent.

5 Section 73(3) also applies and states:

The comptroller shall not take action under subsection (2) above before -

(a) the end of the period for filing an opposition to the European patent (UK) under the European Patent Convention, or

(b) if later, the date on which opposition proceedings are finally disposed of;

and he shall not then take any action if the decision is not to maintain the European patent or if it is amended so that there are not two patents in respect of the same invention.

6 The opposition period referred to in section 73(3)(a) has ended and no opposition was filed, hence Section 73(2) prevails.

7 Furthermore, the Act requires that "invention" in section 73(2) and elsewhere, be understood with reference to section 125(1), which states:

For the purposes of this Act an invention for a patent for which an application has been made or for which a patent has been granted shall, unless the context otherwise requires, be taken to be that specified in a claim of the specification of the application or patent, as the case may be, as interpreted by the description and any drawings contained in that specification, and the extent of the protection conferred by a patent or application for a patent shall be determined accordingly.

8 Thus an invention is defined by the claims, interpreted in light of the specification as a whole. The phrase "for the same invention" in section 73(2) is regarded as embodying the long standing principle that the same monopoly should not be granted twice over.

9 It is generally accepted that section 73(2) covers not only the situation where respective applications contain claims explicitly including all of the same features (including the case where these are claims dependent on quite distinct main claims) but also where the claims differ in their wording but their scope does not differ in substance.

10 As permitted under section 73(2), the applicant has taken the opportunity of making observations and proposed amendments. Section 76(3) deals with post-grant amendments and states:

No amendment of the specification of a patent shall be allowed under section 27(1), 73 or 75 if it -

(a) results in the specification disclosing additional matter, or

(b) extends the protection conferred by the patent.

11 Before the issue of conflict under section 73(2) can be decided, it is necessary to decide whether the amended claims are allowable under section 76(3).

The invention

12 The invention relates to controlling power consumption of a computer processor in order to mitigate problems associated with power dissipation. This is done by monitoring the estimated power consumption of the processor and comparing it with a threshold power consumption. In response to this comparison, a throttling circuit can adjust the performance of the processor, for example by reducing instruction flow in the processor. In other words, if the processor is at risk of overheating by working intensively, the invention reduces the rate of work in order to allow the processor to cool down.

The proposed amendments

13 The proposed amended claims define a processor and a method for controlling a processor, which monitors the *total power consumption of multiple pipelines* within respective *multiple execution cores* of the processor. A *shared digital throttle reduces the instruction throughput* by the processor if the total power consumed should exceed a threshold. The italicised features are the principle features distinguishing the amended claims from those of the granted GB patent.

Construing the proposed amended claims

14 Claim 1 of the granted GB patent as proposed to be amended reads as follows:

A processor comprising:

multiple execution cores each execution core including functional units that form a respective execution pipeline; respective gating circuits to control power delivery to the functional units and to provide signals that indicate power levels delivered to the respective functional units; a shared digital throttle arranged to estimate the total power consumption of functional units in all the pipelines from the provided signals and to compare the estimated total power level of the functional units with a threshold total power level; and to reduce instruction flow in the processor if the estimated total power level exceeds the threshold total power level.

15 Claim 2 of the granted GB patent as proposed to be amended reads as follows:

A method for controlling power consumption in a multiple execution core processor, each execution core including functional units that form a respective execution pipeline, the method comprising:

collecting power signals from respective gating circuits in the processor, the power signals indicating power levels currently delivered to respective functional units associated with the gating circuits; a shared digital throttle determining an estimated total power consumption according to the collected

power signals from the multiple execution cores; comparing the estimated total power consumption level of all the pipelines with a threshold total power consumption level; and reducing an instruction execution rate by the processor when the estimated total power consumption level exceeds the threshold total power consumption level.

16 The current authority on claim construction is found in *Kirin-Amgen Inc v Hoechst Marion Roussel Ltd* [2005] RPC 9[1], where Lord Hoffman held that "When applying a "purposive construction", the question is always what the person skilled in the art would have understood the patentee to be using the language of the claim to mean".

17 In both of the proposed amended claims, each execution core includes functional units that form a respective execution pipeline. Signals indicating power levels being delivered to respective functional units are used by a shared digital throttle to determine an estimated total power consumption by all of the (functional units in all the [claim 1]) pipelines. The shared digital throttle then compares the estimated total power consumption with a threshold total power consumption level and reduces an instruction flow (claim 1) or execution rate (claim 2) of the processor if the estimated total power consumption exceeds the threshold.

18 The *shared digital throttle* is not clearly defined in the claims alone. What is it shared between? It is called a 'throttle', but it is defined in claims 1 and 2 as estimating and comparing power consumption and dependent thereon, reducing (throttling) the instruction throughput. In the description on page 13 describing the multiple execution core processor embodiments, there are inconsistencies between the numbering of Figures 6A and 6B and the description. For example, the shared digital throttle is referenced only once, in the description on page 13, as feature 650 in Figure 6A, but numeral 650 is absent from Figure 6A.

19 If, in an effort to resolve these inconsistencies, a skilled reader were to turn to Figure 1 and the accompanying description on page 5, he would conclude that the digital throttle referred to elsewhere is associated with a single execution core. It then follows that the *shared digital throttle* is shared between multiple execution cores and is operable to reduce the instruction throughput by the multiple execution core processor as whole, but not by individual execution cores (that is the subject of the embodiment of figure 6B, which provides a digital throttle for each execution core). As the description elsewhere supports, the digital throttle may also estimate and compare, or monitor, power levels.

20 On balance, when considered in light of the whole description, I consider the proposed amended claims to clearly define the invention. The skilled person would understand that the shared digital throttle is shared between multiple pipelines and correspondingly between multiple execution cores. The purposive construction they would apply is consistent with the embodiment of the invention described on page 13 of the GB patent, which states '*A shared digital*

[1] *Kirin-Amgen Inc v Hoechst Marion Roussel Ltd* [2005] RPC 9

throttle 650 monitors and adjusts activity in functional units 630 of all pipelines 640'.

21 In the description the term *instruction throughput* covers both *instruction flow* (claim 1) and *instruction execution rate* (claim 2). At page 12 the specification describes reducing *instruction throughput* to cover a number of mechanisms for reducing the rate at which instructions are executed, for example by injecting bubbles into the execution pipeline, and by reducing the frequency of the processor's clock. I have also used the term *instruction throughput* to cover both *instruction flow* and *instruction execution rate*.

The scope of the proposed amended claims – section 76(3)

22 I shall first examine the scope of the claims under section 76(3)(b). If the proposed amended claims do not extend the protection conferred, they are likely to satisfy section 76(3)(a) as long as they are supported by the description.

23 The applicant's observation in their attorney's letter states:

> *The amended claims are limited to a processor with multiple execution cores each execution core including functional units that form a respective execution pipeline and, in accordance with s. 76(3)(b), the amended claims therefore restrict, rather than extend, the protection conferred by the granted UK patent.*

24 I understand this line of reasoning to mean that because the granted claims relate to a processor which is not limited to one execution core, the amended claims must fall within their scope. That is to say, the granted claims cover a processor with at least one execution core and associated features and therefore cover a processor with more than one execution core. A multiple execution core processor which comprises each of the features defined in the granted claims would fall within their scope. This seems prima facie to be a reasonable argument.

25 There are three independent claims in the GB patent which read:

> Claim 1
>
> *A processor comprising*:
>
> *a functional unit;*
>
> *a gating circuit to control power delivery to the functional unit and to provide a signal that indicates a power level delivered to the functional unit;*
>
> *a monitor circuit to compare the indicated power level with a threshold power level; and*
>
> *a throttle circuit to adjust instruction flow in the processor if the indicated power level exceeds the threshold level.*
>
> Claim 7

A method for controlling power consumption in a processor comprising:

collecting power signals from gating circuits in the processor, the power signals indicating power levels currently delivered to functional units associated with gating circuits;

adjusting an indicated power consumption according to the collected power signals;

comparing the indicated power consumption level with a threshold power consumption level; and

adjusting an instruction execution rate by the processor when the accumulated indicated power consumption level exceeds the threshold power consumption level.

Claim 12

A processor comprising:

one or more functional units; and

a digital throttle to monitor activity states of the one or more functional units to indicate a power consumption level for the processor, wherein the digital throttle comprises:

one or more gate units, each gate unit to control power delivery to an associated one of the functional units and to indicate an activity state for the associated functional unit; and

a monitor circuit to determine the processor's power consumption level from the indicated activity states of the one or more functional units.

26 To determine whether the amended claims are allowable under section 76(3)(b), the questions are:

(i) Does the processor of amended claim 1 fall within the scope of either of granted independent claims to a processor 1 or 12?

(ii) Does the method of amended claim 2 fall within the scope of granted independent method claim 7?

27 Claim 12 is the broadest claim of the GB patent and is not limited to reducing the instruction throughput of the processor in dependence upon the comparison of the processor's power consumption with a threshold (the 'throttling' aspect). It therefore makes sense to consider the scope of this claim first. The claim defines a processor comprising one or more functional units, one or more gate units to control power delivery to an associated functional unit and a digital throttle comprising a monitor circuit to determine the processor's power consumption from indicated states of the functional units provided by the associated gate units.

28 In comparison with claim 12, proposed amended claim 1 further specifies that the processor is a multiple execution core processor, capable of processing multiple pipelines. The digital throttle is shared between the execution cores – an arrangement which is not precluded by the scope of granted claim 12. The estimation (totalling), comparison and reduction (throttling) features of proposed amended claim 1 also narrow its scope within the scope of granted claim 12. Having established that proposed amended claim 1 is narrower than that of claim 12 and so is allowable under section 76(3)(b), it is not necessary to also consider its scope against that of granted claim 1.

29 Turning to the question of proposed amended claim 2, granted claim 7 covers plural power signals from plural gating circuits in association with plural functional units. An indicated power consumption is adjusted according to the *collected* power signals and is compared with a threshold power consumption level. Claim 7 specifies that an instruction execution rate is adjusted when the *accumulated* indicated power consumption level exceeds the threshold. This means that the only method claimed in the granted GB patent is limited to adjusting an instruction execution rate by the processor in dependence upon an *accumulated* power consumption level. What does this mean in comparison with proposed amended claim 2?

30 Construction of claim 7 is frustrated because it is not immediately clear how the *collected* power signals relate to the indicated power consumption - are they simply *totalled*?; what manner of adjustment is performed on the indicated power consumption?; it is unclear whether the indicated power consumption is the same as the *accumulated* indicated power consumption (which otherwise carries no antecedent).

31 Turning to the description, the skilled reader would understand that whilst 'collecting' power signals may include totalling them as defined in proposed amended claim 2, obtaining an *accumulated indicated power consumption level* involves an extra step. The description of the GB patent is of assistance here. At page 4 line 31 to page 5 line 7 the patent describes how the power signals for active functional units may be summed. In one embodiment these clock by clock estimates may be accumulated over multiple clock cycles to provide an accumulated power value – accumulated over time. The skilled reader then would understand that claim 7 is limited to adjusting the instruction throughput dependent upon an *accumulated indicated power consumption level*, and that it is a particular, narrower, embodiment of the 'estimated total power level' of amended claim 2. Proposed claim 2 does not then, in this aspect, fall within the scope of granted claim 7 and so would extend the protection conferred by the GB patent.

Whether the claims define additional matter – section 76(3)(a)

32 I have determined that proposed amended claim 2 is not allowable under section 76(3)(b) and so it is unnecessary to also consider it under section 76(3)(a). However, by extension, the discussion of claim 1 will apply to equivalent substantive features of claim 2.

33 In assessing whether or not amendments disclose additional matter under section 76(3)(a), comparison is to be made with the application as filed[2]. The applicant's observations in their attorney's letter of 29th May 2012 are succinct, and refer to Figure 6A and the corresponding description on page 13 lines 8-15 for "particular basis and support".

34 When construing the proposed amended claims above, I found support for the proposed amendments in the specification: Reference to the embodiment of figure 6A, described on page 13 of the application as filed, teaches a skilled reader that one embodiment of the invention relates to a multiple execution core processor. By also referring to the description elsewhere, a skilled person would understand that a shared digital throttle monitors and adjusts activity in associated pipelines to control the total power consumption within a threshold.

35 Consequently proposed amended claim 1 does not define additional matter, over the application as filed, under section 76(3)(a).

Does the amended GB patent define the same invention as the EP patent?

36 The applicant's observations, in their attorney's letter of 29th May 2012, draw a distinction between the amended claims of the GB patent and the granted claims of the EP patent on the basis that they include "a feature of a digital throttle shared between multiple pipelines". The letter then outlines the advantage of this arrangement over the embodiment shown in Figure 6B of the patent which discloses not a *shared digital throttle* but a digital throttle for each execution core. The letter also cites *Marley's Patent* [1994] RPC 231[3] as the correct authority to apply in determining conflict of claims.

37 The letter argues that "merely replacing a generic feature of the UK claims by an embodiment of that feature" will not overcome double patenting, but that "adding a new essential feature to the UK claims" may overcome conflict. The *shared digital throttle* is, the applicant argues, just such a feature.

38 *Marley's Patent* is helpful here. At lines 40 to 45 on page 240 of the RPC Balcombe LJ states:

> *How then should section73(2) be construed? It seems to me that the obvious purpose of the sub-section is to enable the Comptroller to prevent there being in existence two patents for the same invention, having the same priority date, and where the applications for both patents were filed by the same applicant, and this irrespective of the fact that other linked inventions may be included in the claims of either patent.*

39 At lines 5-8 of page 241 of the RPC, he states:

> *In my judgement the correct construction of the sub-section is the literal one. If the claims of the U.K. patent and the European patent cover the same*

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[2] *Merrell Dow Pharmaceuticals Inc v H N Norton & Co Ltd* (BL C/089/96) Manual of Patent Practice 76.25

[3] *Marley's Patent* [1994] RPC 231

invention, whatever other linked inventions may be covered by the claims of either patent, then the Comptroller may revoke the U.K. patent.

40 In *SeeReal Technologies* (BL O/261/12)[4], the Hearing Officer, Dr. Stephen Brown, also referred to *Marley's Patent* and helpfully considered the issue of claims defining more than one invention. At para. 30 and 31 he states:

"The fact that if feature 'B' had been in the parent it would have been a perfectly acceptable dependent claim does not automatically mean that it must conflict if present in a second application. Put another way, the absence of plurality does not necessarily mean the presence of conflict. Section 14(5)(d) of the Act states:

The claim or claims shall –

….

(d) relate to one invention or to a group of inventions which are so linked as to form a single inventive concept

The Act thus recognises that one application may acceptably contain several different inventions so long as they fall within the same inventive concept. This is in contrast to Section 18(5) which, as quoted above, is concerned with whether or not the *same invention* is present in two or more applications. Thus it seems to me that it is entirely possible for features 'A' & 'B' to fall within the same inventive concept while relating to different inventions."

41 This, in effect, is on all fours with the applicant's 'new essential feature' argument. The test for conflict is not whether two patents define the same inventive concept, but whether the claims in each patent, when properly construed, define the same invention.

42 The EP patent comprises two independent claims:

Claim 1:

A processor comprising:

functional units to form an instruction execution pipeline for the processor; an instruction delivery system to provide instructions to the instruction execution pipeline; ***characterised by*** *gating circuits to control power delivery to the functional units and to provide signals that indicate power levels delivered to the functional units; a monitor circuit to compare an estimated power consumption level, according to the indicated power levels with a threshold power level; and a throttle circuit to adjust instruction flow in the processor when an accumulated estimated power consumption level for a number of cycles of a processor clock exceeds the threshold power consumption level.*

Claim 4:

[4] *SeeReal Technologies* (BL O/261/12)

A method for controlling power consumption in a processor comprising:

collecting power signals from gating circuits in the processor, the power signals indicating power levels currently delivered to functional units associated with the gating circuits, wherein the gating circuits are arranged to control power delivery to the functional units; providing instructions from an instruction delivery system to an instruction execution pipeline, wherein the functional units form the instruction execution pipeline for the processor; adjusting an estimated power consumption according to the collected power signals; comparing the estimated power consumption level with a threshold power consumption level; and adjusting an instruction execution rate by the processor when an accumulated estimated power consumption level for a number of cycles of a processor clock exceeds the threshold power consumption level.

43 The independent claims of the EP patent do not present any difficulties of construction. The claims only define a single execution pipeline. Whilst this does not preclude a multiple execution core processor falling within the scope of the claims, the characterising features do not point towards its inclusion. The claims, I think, are written with only a single pipeline in mind and I believe a skilled person would come to the same conclusion.

44 In construing the 'accumulation' feature defined in the claims, a skilled person would turn to the description. In accordance with section 125(1) and *Kirin-Amgen*[5], I too must do so. The specification teaches that an accumulated power value may be estimated over multiple clock cycles that smoothes out clock by clock variations in the processor's power consumption.

45 This contrasts with a purposive construction of proposed amended claim 1. That claim is limited to estimating and comparing the *total power level* of the multiple execution core processor by throttling multiple execution cores simultaneously. This aspect is different in scope, and is for a different purpose, than the *accumulated* limitation of the EP patent.

46 I have construed proposed amended claim 1 of the GB patent and the granted claims of the EP patent to define two separate inventions:

- The amended GB patent defines controlling power consumption in a multiple execution core processor by estimating the total power level in all execution core pipelines and using a shared digital throttle to reduce instruction throughput in the processor if the total power level exceeds a threshold. This means that each execution core can borrow power from the remaining execution cores as long as the total power threshold is not exceeded.

- The EP patent defines controlling power consumption in a processor by accumulating the estimated power levels of functional units forming a pipeline over a number of cycles of a processor clock and using a (digital) throttle to adjust instruction throughput if the accumulated estimated

[5] Kirin-Amgen Inc v Hoechst Marion Roussel Ltd [2005] RPC 9

power level exceeds a threshold. This means that clock by clock variations in the processor's power consumption are smoothed out.

Conclusion

47 I have found that proposed amended claim 1 of the GB patent is allowable under section 76(3)(b), but that proposed amended claim 2 extends the protection conferred and is not allowed.

48 I went on to find that proposed amended claim 1 of the GB patent does not define additional subject matter under section 76(3)(a) and is allowed. I did not consider proposed amended claim 2 as it did not pass the test under section 76(3)(b).

49 Because proposed amended claim 2 is not allowable, I have only considered proposed amended claim 1 under section 73(2) and found that it does not define the same invention as the EP patent.

50 Consequential amendments to the description and current proposed amended claims will be necessary in order to resolve the outstanding issues. When making such amendments, the requirement for any amended method claim not to extend the protection conferred beyond the *accumulated indicated power consumption level* limitation of granted claim 7 should be observed. I note that the claims of the EP patent are also limited to an *accumulated* power consumption level and care should be taken that any new amendments do not define the same invention as the EP patent.

51 Upon receipt of those amendments the application will be remitted to the Examiner for processing. I hereby give the applicant 1 month from the date of this decision to submit the necessary amendments or the GB patent will be revoked.

Appeal

52 Under the Practice Direction to Part 52 of the Civil Procedure Rules, any appeal must be lodged within 28 days.

Ben Buchanan

Deputy Director, acting for the Comptroller